

FIG. 1

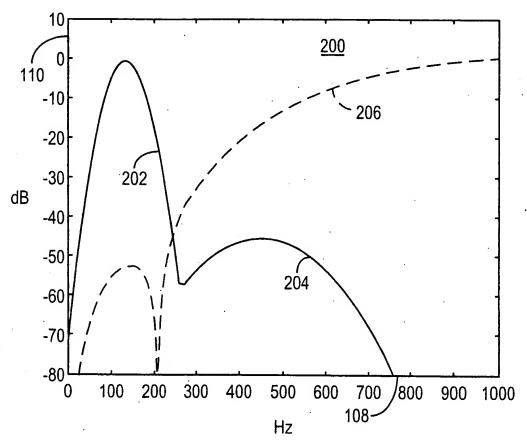


FIG. 2

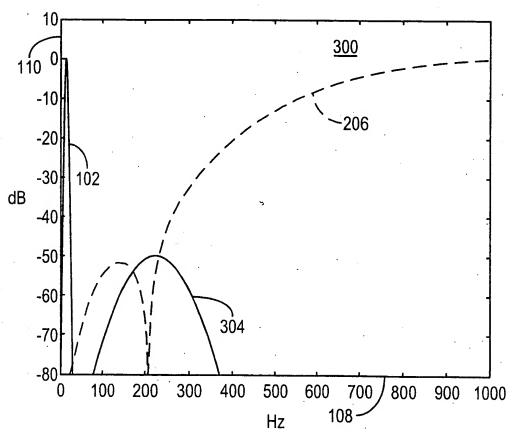


FIG. 3

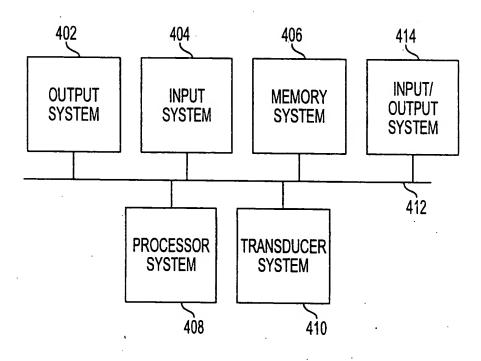


FIG. 4

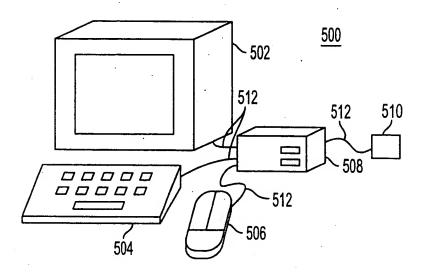


FIG. 5

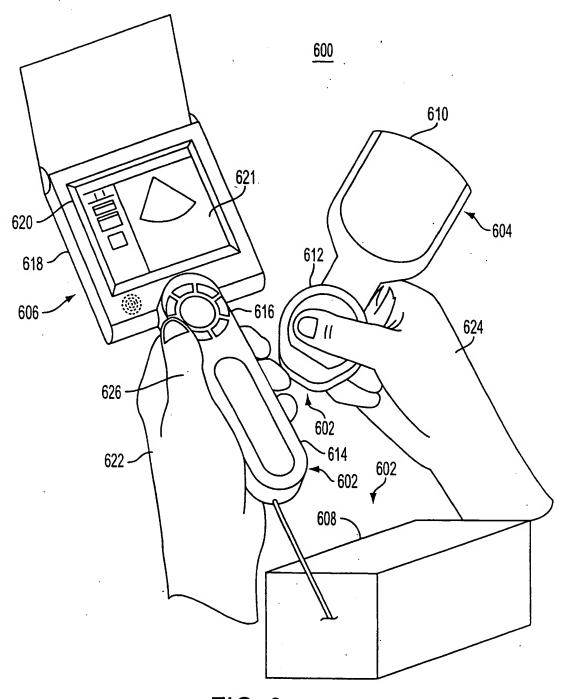


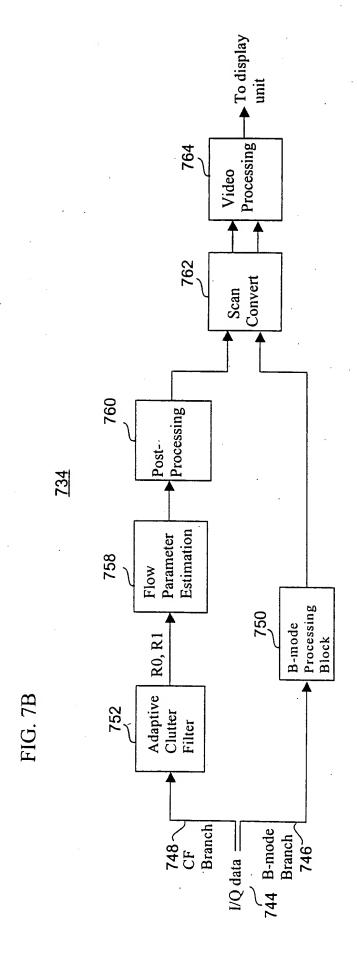
FIG. 6

730 Display Unit 734 Image processor 738 <u>S</u> 744 732 Master Controller Memory Buffer 726 404 716 Area Former Input System Receive channels Transmitter 7,13 712 210

FIG. 7A

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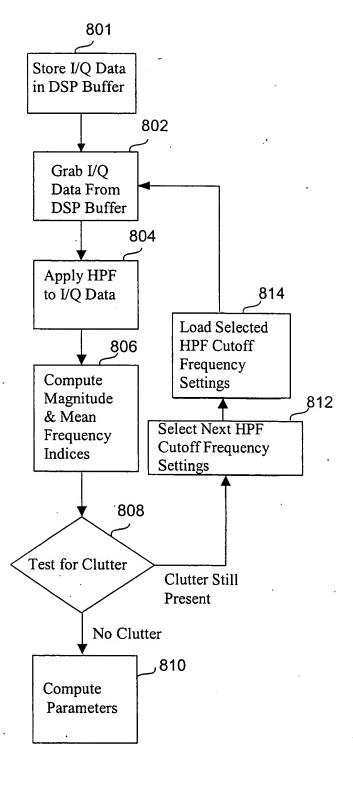


FIG. 8

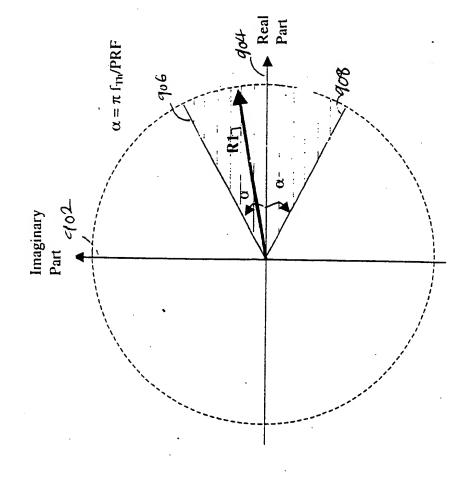


FIG. 9